Notice of References Cited	Application/Control No. 10/616,021	Applicant(s)/Patent Under Reexamination LEE ET AL.	
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U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-			
	B	US-			
	C	US-			
	D	US-			
	E	US-			
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FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	"A 6Gbps CMOS Phase Detecting DEMUX Module Using Half-Frequency Clock", Nakamura et al, IEEE 1998 Symposium on VLSI Circuits Digest of Technical Papters, pp/ 196-197
	V	"A 4-Gb/s Clock and Data Recoveyr Circuit Using Four-Phase 1/8-Rate Clock", Song et al, Proceedings of the 28th Solid-State Circuits Conference, 24-26 Sept 2002 ESSCIRC2002, pp. 239-242
*	W	"A 10Gb/s CMOS Clock and Data Recovery Circuit with Frequency Detection", Savoj et al, 2001 IEEE International Solid-State Circuits Conference, Digest of Technical Papters, February 2001
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.